Docket No.: 524322000300
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:
Dennis CIPLICKAS et al.

Application No.: 10/538,538 Confirmation No.: 4236

Filed: December 11, 2003 Art Unit: 2891

For: FAST LOCALIZATION OF ELECTRICAL FAILURES OF AN INTEGRATED CIRCUIT SYSTEM AND METHOD Examiner: I. U. Anya

APPEAL BRIEF

MAIL STOP: APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on May 27, 2008. The fees required under 37 C.F.R. § 41.20(b)(2) and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

PDF Solutions, Inc., a California corporation, with a principal place of business in San Jose, California.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 56 claims pending in the present application.

B. Current Status of Claims

1. Claims canceled: 5 and 32.
2. Claims withdrawn from consideration but not canceled: None.
3. Claims pending: 1-4, 6-31, and 33-58.
4. Claims allowed: None.
5. Claims rejected: 1-4, 6-31, and 33-58.
6. Claims objected to: None.

C. Claims on Appeal

The claims on appeal are claims 1-4, 6-31, and 33-58.

IV. STATUS OF AMENDMENTS

No Amendments remain outstanding.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a method for fast localization of electrically measured defects of integrated circuits. (Page 1, paragraph [0002]; page 3, paragraph [0033]; Figure 1.) A test chip is obtained. (Page 6, paragraphs [0048], lines 1-3.) The test chip is fabricated to have test structures configured for parallel electrical testing. (Page 4, paragraph [0036], lines 1-2; page 7, paragraph [0051], lines 1-3; Figure 6.) The test chip test structures are grouped into one or more padgroups. (Page 4, paragraph [0037], lines 2-3; page 7, paragraph [0051], lines 4-8; Figure 6.) The test structures in a padgroup are electrically tested together in parallel. (Page 4, paragraph [0037], lines 4-5; page 7, paragraph [0053], lines 1-3) The test structures on the test chip are tested using a parallel electrical tester. (Page 7, paragraph [0054], line 1-2; page 15, paragraphs [0091]-[0093]; Figure 23; Figure 24.) The results of the electrical testing are analyzed to localize defects on the test chip. (Page 4, paragraph [0040]; page 20, paragraph [00111].)

Independent claim 28 recites a system for fast localization of electrically measured defects of integrated circuits. (Page 1, paragraph [0002]; page 3, paragraph [0033]; Figure 1.) A test chip is obtained. (Page 6, paragraphs [0048], lines 1-3.) The test chip is fabricated to have test structures configured for parallel electrical testing. (Page 4, paragraph [0036], lines 1-2; page 7,

paragraph [0051], lines 1-3; Figure 6.) The test chip test structures are grouped into one or more padgroups. (Page 4, paragraph [0037], lines 2-3; page 7, paragraph [0051], lines 4-8; Figure 6.) The test structures in a padgroup are electrically tested together in parallel. (Page 4, paragraph [0037], lines 4-5; page 7, paragraph [0053], lines 1-3) The test structures on the test chip are tested using a parallel electrical tester. (Page 7, paragraph [0054], line 1-2; page 15, paragraphs [0091]-[0093]; Figure 23; Figure 24.) The results of the electrical testing are analyzed to localize defects on the test chip. (Page 4, paragraph [0040]; page 20, paragraph [00111].)

Independent claim 58 recites a computer readable medium containing computer executable doe for fast localization of electrically measured defects of integrated circuits. (Page 1, paragraph [0002]; page 3, paragraph [0033]; Figure 1.) A test chip is obtained. (Page 6, paragraphs [0048], lines 1-3.) The test chip is fabricated to have test structures configured for parallel electrical testing. (Page 4, paragraph [0036], lines 1-2; page 7, paragraph [0051], lines 1-3; Figure 6.) The test chip test structures are grouped into one or more padgroups. (Page 4, paragraph [0037], lines 2-3; page 7, paragraph [0051], lines 4-8; Figure 6.) The test structures in a padgroup are electrically tested together in parallel. (Page 4, paragraph [0037], lines 4-5; page 7, paragraph [0053], lines 1-3) The test structures on the test chip are tested using a parallel electrical tester. (Page 7, paragraph [0054], line 1-2; page 15, paragraphs [0091]-[0093]; Figure 23; Figure 24.) The results of the electrical testing are analyzed to localize defects on the test chip. (Page 4, paragraph [0040]; page 20, paragraph [00111].)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1-2, 12-15, 26-29, 39-42, and 56-58 are unpatentable under 35 USC 102(b) over U.S. Patent No. 5,831,446 (the So reference).

B. Whether claims 3, 4, 30, 31, and 43-45 are unpatentable under 35 USC 103(a) over the So reference in view of U.S. Patent No. 6,201,254 (the Chou reference).

C. Whether claims 6-11, 18-20, 33-38, and 48-50 are unpatentable under 35 USC 103(a) over the So reference in view of U.S. Patent 5,666,049 (the Yamada reference).

D. Whether claims 16, 17, 46, and 47 are unpatentable under 35 USC 103(a) over the So reference in view of U.S. Patent Application Publication No. 2004/0094762 (the Hess reference).

E. Whether claims 21-25 and 51-55 are unpatentable under 35 USC 103(a) over the So reference in view of the Yamada reference and in further view of U.S. Patent No. 6,323,664 (the Kim reference).

VII. ARGUMENT

Applicants respectfully request reversal of the Examiner's rejection of claims 1-4, 6-31, and 33-58 in view of the following remarks.

A. Whether claims 1-2, 12-15, 26-29, 39-42, and 56-58 are unpatentable under 35 USC 102(b) over U.S. Patent No. 5,831,446 (the So reference).

1. Claims 1, 28, and 58

Independent claims 1, 28, and 58 recite, "the test structures in a padgroup are electrically tested together in parallel."

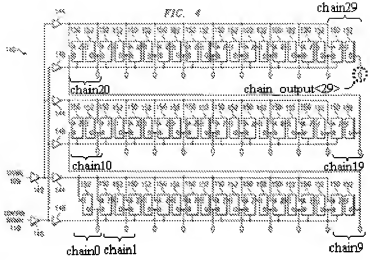
As noted by Applicants during prosecution, the term "parallel" could have two possible meanings: one meaning is electrical (i.e., two test structures are connected electrically in parallel such that the output of one is not the input of another); and another meaning is temporal (i.e., two test structures are tested at approximately the same time). These two meanings are not synonymous and should not be conflated. In other words, testing two test structures connected electrically in parallel does not necessarily require that they be tested at approximately the same time. For example, assume that two test structures are connected electrically in parallel (i.e., the output of one test structure is not the input of another test structure). One of the two test structures can be tested at one time, and then the other test structure can be tested at a later time. In this example, the two test structures are tested in parallel because the two test structures are connected electrically in parallel (i.e., the output of one test structure is not the input of another test structure) even though they were tested at different times.

In the present application, independent claims 1, 28, and 58 explicitly recite that the test structures in a padgroup are electrically tested "**together in parallel**." Thus, the term "**together**" requires that the test stuctures in the padgroup are tested at approximately the same time, while the term "**parallel**" requires the test structures are connected electrically in parallel when they are tested at approximately the same time.

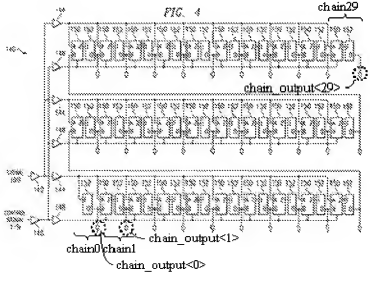
Applicants have asserted that the So reference only uses the term "parallel" consistent with the electrical meaning (i.e., that the chains are connected electrically in parallel). In particular, FIG. 4 of the So reference depicts 30 chains, which are tested in series and in parallel.

When tested in series, the output of one chain is connected to the input of a subsequent chain, which is consistent with the electrical meaning of the term "series." For example, as shown in the annotated copy of FIG. 4 below, the output of chain0 is connected to the input of chain1 through input "B" of multiplexing element 150 of chain1. Similarly, the output of chain9 (last chain in first row) is connected to the input of chain10 (first chain in second row); and the output of chain19 (last chain in second row) is connected to the input of chain20 (first chain in third row). Because the 30 chains are connected in series, the entire chain of 30 chains is tested by reading from

the output of the last chain (i.e., chain_output<29> of chain 29). Thus, if there is any fault in any one or more of the chains, then the fault can be detected by reading chain_output<29>.



When tested in parallel, each input of each chain is provided by signal 109 through input "A" of multiplexing element 150 rather than receiving the output of a previous chain through input "B" of multiplexing element 150, which is consistent with the electrical meaning of the term "parallel." The output of each chain is tested using an output pad for each output signal. For example, as shown in the annotated copy of FIG. 4 below, the output of chain0 is tested using an output pad for chain_output<0>; and the output of chain1 is tested using a separate output pad for chain_output<1>. Thus, each chain is tested by reading the individual output for each of the chain.



The So reference does not disclose arranging the output pads of the chains into pad groups to allow for multiple outputs of multiple chains to be read at approximately the same time. Instead, each output pad is depicted separated from one another. For example, as shown above in the annotated version of FIG. 4, the output pad for chain0 labeled with output_signal<0> is separated from the output pad of chain1 labeled with output_signal<1>. No group of output pads are shown as being arranged in a pad group that would allow for the output pads to be tested together (at approximately the same time).

In the Advisory Action the Examiner asserts that "the thirty chains [of Figure 4] are grouped into three pad groups (Chains 0-9, chains 10-19 and chains 20-29) and the groups are tested separately and contemporaneously in parallel as three groups." The Examiner, however, fails to cite to any support for the Examiner's assertion. Instead, as detailed above, Applicants assert that the So reference discloses only two modes for testing chains 0-29 (serial and parallel modes). In the serial mode, chains 0-29 are all tested together in series by reading from the output of the last chain (chain_output<29> of chain29). In the parallel mode, each chain is tested separately in parallel by reading from the output of each chain separately. The So reference does not disclose any sub grouping of multiple chains of chains 0-29 being tested separately and in parallel, such as chains 10-19 being tested separately from and in parallel with chains 0-9 or chains 20-29. Indeed, it is not obvious how such a test could be performed since chain 10 receives as an input either the output of chain 9 (in the serial mode) or the same input from signal 109 as all other chains (in the parallel mode).

Moreover, Applicants assert that the So reference teaches away from testing the chains at approximately the same time when they are connected electrically in parallel because testing the chains at approximately the same time makes the serial mode redundant. In particular, in the So reference, the serial mode is used to quickly test all 30 chains together at the same time using one output (chain_output<29>). If the chain of 30 chains passes the serial mode test, then all 30 of the chains in the chain are good because they are connected in series. In this case, there is no need to perform the parallel mode test. If the chain of 30 chains fails the serial mode test, then one or more of the 30 chains is bad, but it is not known from the serial mode test which one(s) because they are

connected in series. In this case, the parallel mode test is needed to test each chain one at a time to pinpoint the bad chain(s). Thus, the purpose of the serial test mode, which allows all 30 chains to be tested together at the same time, is to avoid having to test each chain one at a time during the parallel test mode, which is time consuming. If all 30 chains could be tested together at the same time during the parallel test mode, then the serial test mode would not be necessary.

Thus, Applicants assert that claims 1, 28, and 58 are allowable over the So reference.

2. Claims 2 and 29

Claims 2 and 29 recite "**inspecting the localized defects** on the test chip using an inspection tool." (Emphasis added.) The Examiner cites to column 2, lines 36-39 of the So references as disclosing these elements. The So reference discloses "pop-up observation points . . . [which] provide observability and probing of the **inverter cells** through via 1-2-3 by e-beam." (Emphasis added; column 2, lines 36-39.) Specifically, an e-beam is used to observe "[t]he **signal** at the pop-up" points." (Emphasis added; column 2, line 67.) Thus, the So reference discloses **observing the inverter signal** and **probing the inverter cells** at the pop-ups. Therefore, the So reference does not disclose "**inspecting the localized defects** on the test chip using an inspection tool," as recited by claims 2 and 29. For at least this reason, Applicants respectfully assert that claims 2 and 29 are allowable over the So reference.

Additionally and alternatively, Applicants assert that claims 2 and 29, which depend on claims 1 and 28 respectively, are allowable for at least the reason that they depend from allowable independent claims.

3. Claims 12 and 39

Claims 12 and 39 recite "in-line inspecting the test chip using an optical inspection tool." The Examiner cites to column 4, lines 52-62 of the So reference as disclosing these elements. The cited passage discloses monitoring process shifts and process related manufacturing defects by testing a test chip, which is manufactured along side other products. (Column 4, lines 52-62.) The So reference does not disclose, in the Examiner cited passage, "in-line inspecting the test chip using

an optical inspection tool," as recited by claims 12 and 39. For at least this reason, Applicants respectfully assert that claims 12 and 39 are allowable over the So reference.

Additionally and alternatively, Applicants assert that claims 12 and 39, which depend on claims 1 and 28 respectively, are allowable for at least the reason that they depend from allowable independent claims.

4. Claims 14 and 40

Applicants assert that claims 14 and 40, which depend on independent claims 1 and 28 respectively, are allowable for at least the reason that they depend on allowable independent claims.

5. Claims 15 and 42

Claims 15 and 42 recite that "one of the test structures is a snakecomb cell." An example of a snakecomb cell is shown in Figure 12A of the present application. Paragraph [0050] of the present application describes an example of a snakecomb as having "[v]ertical or horizontal metal lines arranged in a 'grating.'"

The Examiner cites to Figure 1 of the So reference as disclosing claims 15 and 42. Figure 1 is a shematic of the test circuitry used in the test chip. (Column 2, lines 27-29.) The circuitry consists of inverters and "a path through the different metal layers." (Column 2, lines 32-36, lines 57-58.) Therefore, the So reference does not disclose, in the Examiner cited passage, "a snakecomb cell," as recited by claims 15 and 42. For at least this reason, Applicants respectfully assert that claims 15 and 42 are allowable over the So reference.

Additionally and alternatively, Applicants assert that claims 15 and 42, which depend on claims 1 and 28, respectively, are allowable for at least the reason that they depend from allowable independent claims.

6. Claims 26 and 56

Claims 26 and 56 recite, "classifying detected defects as random or systematic defects." The Examiner cites to column 4, lines 52-62 of the So reference as disclosing the elements of these claims. The cited passage discloses tracking "process-related manufacturing defects" to be used for process improvement (column 4, lines 52-55.) The passage does not discuss classifying different types of process-related manufacturing defects. Therefore, So does not disclose, in the Examiner cited passage, "classifying detected defects as random or systematic defects," as recited by claims 26 and 56. For at least this reason, Applicants respectfully assert that claims 26 and 56 are allowable over the So reference.

Additionally and alternatively, Applicants assert that claims 26 and 56, which depend on claims 1 and 28, respectively, are allowable for at least the reason that they depend from allowable independent claims.

7. Claims 27 and 57

Claims 27 and 57 recite, "grouping test chip design patterns into layout bins." The Examiner cites to column 4, lines 52-62 of the So reference as disclosing these elements. The cited passage discloses that monitoring process shifts and tracking process-related manufacturing defects so that yield on products can be improved. (Column 4, lines 52-55.) Additionally, the So reference discloses only one test chip design. (Column 2, lines 31-32.) Thus, the So reference, in the Examiner cited passage, does not disclose "grouping test chip design patterns into layout bins," as recited by claims 27 and 57. For at least this reason, Applicants assert that claims 27 and 57 are allowable over the So reference.

Additionally and alternatively, Applicants assert that claims 27 and 57, which depend on claims 1 and 28, respectively, are allowable for at least the reason that they depend from allowable independent claims.

B. Whether claims 3, 4, 30, 31, and 43-45 are unpatentable under 35 USC 103(a) over the So reference in view of U.S. Patent No. 6,201,254 (the Chou reference).

Applicants assert that claims 3, 4, 30, 31, 43, 44, and 45, which variously depend on independent claims 1 and 28, are allowable for at least the reason that they depend on allowable independent claims.

C. Whether claims 6-11, 18-20, 33-38, and 48-50 are unpatentable under 35 USC 103(a) over the So reference in view of U.S. Patent 5,666,049 (the Yamada reference).

1. Claims 6 and 33

Claims 6 and 33 recite that "a padgroup includes: two columns of test structures; and two columns of pads disposed between the two columns of test structure." The Examiner cites to Figure 14A of Yamada as disclosing these elements. Figure 14A "is the top view of [a] probe card." (Column 11, line 45.) The probe card is for use with semiconductor test circuit chips, which are illustrated to have pads surrounding the perimeter of the test circuit chips. (Figure 14A.) Because pads on all sides of each test chip are required to test each chip, two columns of these test circuit chips cannot combine to form a padgroup with "pads disposed between the two columns of test structures," as recited by claims 6 and 33. For at least this reason, Applicants assert that claims 6 and 33 are allowable over the combination of the So and Yamada references.

Additionally and alternatively, Applicants assert that claims 6 and 33, which depend on claims 1 and 28, respectively, are allowable for at least the reason that they depend from allowable independent claims.

2. Claims 7, 8, 34 and 35

Applicants respectfully assert that claims 7, 8, 34 and 35, which variously depend on independent claims 1 and 28, are allowable for at least the reason that they depend on allowable independent claims.

3. Claims 9 and 36

Examiner has not discussed claims 9 and 36 in the previous Office Actions.

Claims 9 and 36 recite that, "test structures and corresponding pads are disposed between two padgroups." The test structures "are used to verify the operation of the probe card." Figures 13-15 of the Yamada reference disclose probe cards with pin layouts for 9 test chips. There are no other test chips disclosed between the group of 9 test chips. Thus, the So and Yamada references do not disclose any cells with test structures "between two padgroups." For at least this reason, Applicants assert that claims 9 and 36 are allowable over the combination of the So and Yamada references.

Additionally and alternatively, Applicants assert that claims 9 and 36, which depend on claims 1 and 28, respectively, are allowable for at least the reason that they depend from allowable independent claims.

4. Claims 10 and 37

Examiner has not discussed claims 10 and 37 in the previous Office Actions.

Applicants respectfully assert that claims 10 and 37, which variously depend on independent claims 1 and 28, respectively, are allowable for at least the reason that they depend on allowable independent claims.

5. Claims 11 and 38

Examiner has not discussed claims 11 and 38 in the previous Office Actions.

Neither the So reference nor the Yamada reference disclose "adjusting the number of sticks stacked together in the layout to fit within a scanner view field," as recited by claims 11 and 38. For at least this reason, Applicants assert that claims 11 and 38 are allowable over the combination of the So and Yamada references.

Additionally and alternatively, Applicants assert that claims 11 and 38, which depend on claims 1 and 28, respectively, are allowable for at least the reason that they depend from allowable independent claims.

6. Claims 18 and 48

Claims 18 and 48 recite that, "the parallel electrical tester is connected to **a wafer loader** and a wafer prober." The Examiner cites to Figure 12 of the Yamada as disclosing the elements of these claims. The figure is of "a semiconductor testing apparatus" containing "the main body of a prober, ... the main body of a probe card, ... a plurality of probe needles, a workstation, ... [and] a chuck stage." (Column 10, lines 51-67.) Thus, the Yamada reference does not disclose, in the Examiner cited passage, that "the parallel electrical tester is connected to **a wafer loader** and a wafer prober," as recited by claims 18 and 48. For at least this reason, Applicants assert that claims 18 and 48 are allowable over the combination of the So and Yamada references.

Additionally and alternatively, Applicants assert that claims 18 and 48, which depend on claims 1 and 28, respectively, are allowable for at least the reason that they depend from allowable independent claims.

7. Claims 19, 20, 49 and 50

Claims 19, 20, 49, and 50 recite transmitting signals between a pin termination module and a measurement control module in the parallel electrical tester. The Examiner cites to Figures 5 and 17 of the Yamada reference as disclosing these elements.

Figure 5 shows "a power source . . . which provides power [] to the semiconductor integrated-circuit." (Column 7, lines 15-17.) Thus, Figure 5 discloses a power source. Figure 17 shows an "alignment detecting means . . . by using electrostatic capacity." (Column 13, lines 20-22.)

The Yamada reference discloses controlling the testing apparatus with a work station. (Column 10, line 59-60.) The work station transmits control signals directly to the semiconductor

testing circuit chips on the probe card. Thus, the Yamada reference does not disclose, at the Examiner cited passages, transmitting control signals between a pin termination model and a measurement control module in the parallel electrical tester, as recited by claims 19, 20, 49, and 50. For at least this reason, Applicants assert that claims 19, 20, 49, and 50 are allowable over the combination of the So and Yamada references.

Additionally and alternatively, Applicants assert that claims 19, 20, 49, and 50, which variously depend on claims 1 and 28, are allowable for at least the reason that they depend from allowable independent claims.

D. Whether claims 16, 17, 46, and 47 are unpatentable under 35 USC 103(a) over the So reference in view of U.S. Patent Application Publication No. 2004/0094762 (the Hess reference)

Applicants note that the Hess reference is assigned to PDF Solutions, Inc. The present application was assigned to PDF Solutions, Inc. at the time of filing. Thus, Applicants assert that the Hess reference can not be used as a reference under 35 USC 103. Additionally and alternatively, Applicants assert that claims 16, 17, 46, and 47, which variously depend on claims 1 and 28, are allowable for at least the reason that they depend from allowable independent claims.

E. Whether claims 21-25 and 51-55 are unpatentable under 35 USC 103(a) over the So reference in view of the Yamada reference and in further view of U.S. Patent No. 6,323,664 (the Kim reference).

1. Claims 21 and 51

Claims 21 and 51 recite that "each switch card is connected to **a group of pins** from the probe card." (Emphasis added.) The Examiner cites to Figure 3 of the Kim reference as disclosing these elements. Figure 3 shows "the test chip". (Column 3, line 32.) The circuitry illustrated in Figure 3 is on the test chip. (Figure 3.) Each switching circuit is attached to a buffer (DOUT_BUF0-DOUT_BUF31). Each of the buffers is attached to a single pad (PAD0-PAD31). Pads are illustrated as having a single probe pin (12A-12H) connected to each switching circuit.

Thus, the switching circuits in Figure 3 are, at most, attached to **a single pin**. Therefore, the Kim reference does not disclose, in the cited figure, that "each switch card is connected to **a group of pins** from the probe card," as recited by claims 12 and 51. For at least this reason, Applicants respectfully assert that claims 21, and 51 are allowable over the combination of the So,Yamada, and Kim references.

Additionally and alternatively, Applicants assert that claims 21 and 51, which depend on claims 1 and 28, respectively, are allowable for at least the reason that they depend from allowable independent claims.

2. Claims 22 and 52

Claims 22 and 52 recite forming "a resistor divider with a resistor." The Examiner cites to Figure 4 of the Kim reference as disclosing these elements. Figure 4 is an embodiment of a switching circuit. (Column 5, lines 8-9.) There are no resistors displayed in Figure 4 or discussed in the section describing Figure 4. (Column 5, lines 8-36.) Moreover, resistors are not discussed at all in the Kim reference. Therefore, the Kim reference does not disclose, in the Examiner cited figure, forming "a resistor divider with a resistor," as recited by claims 22 and 52. For at least this reason, Applicants assert that claims 22, and 52 are allowable over the combination of the So,Yamada, and Kim references.

Additionally and alternatively, Applicants assert that claims 22 and 52, which depend on claims 1 and 28, respectively, are allowable for at least the reason that they depend from allowable independent claims.

3. Claims 23-25 and 53-55

Applicants assert that claims 23-25 and 53-55, which variously depend on independent claims 1 and 28, are allowable for at least the reason that they depend on allowable independent claims.

F. CONCLUSION

For at least the forgoing reasons, Applicants request reversal of the Examiner's rejections of claims 1-4, 6-31, and 33-58.

VIII. CLAIMS APPENDIX

A list of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.

REMARKS

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 524322000300. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: August 26, 2008

Respectfully submitted,

By /Peter J. Yim/
Peter J. Yim
Registration No.: 44,417
MORRISON & FOERSTER LLP
425 Market Street
San Francisco, California 94105-2482
(415) 268-6373

APPENDIX A

Claim 1: A method for fast localization of electrically measured defects of integrated circuits, comprising:

(a) obtaining a test chip fabricated to have test structures configured for parallel electrical testing, wherein the test structures are grouped into one or more padgroups, wherein the test structures in a padgroup are electrically tested together in parallel;

(b) electrically testing the test structures on the test chip employing a parallel electrical tester; and

(c) analyzing results of the electrical testing to localize defects on the test chip.

Claim 2: The method of claim 1, further comprising:

inspecting the localized defects on the test chip using an inspection tool.

Claim 3: The method of claim 2, wherein the inspection tool is a scanning electron microscope (SEM).

Claim 4: The method of claim 3, further comprising:

sizing the test structures on the test chip to be compatible with a view field of the SEM.

Claim 5 (Canceled)

Claim 6: The method of claim 1, wherein a padgroup includes:

two columns of test structures; and

two columns of pads disposed between the two columns of test structures.

Claim 7: The method of claim 1, further comprising:

grouping padgroups into one or more sticks, wherein the padgroups in a stick are electrically tested together in parallel.

Claim 8: The method of claim 7, wherein the padgroups in a stick are electrically tested together in parallel using a probe card connected to the parallel electrical tester.

Claim 9: The method of claim 8, wherein one or more cells having test structures and corresponding pads are disposed between two padgroups in a stick, wherein the one or more cells are used to verify the operation of the probe card.

Claim 10: The method of claim 7, further comprising:

stacking two or more sticks together in a layout.

Claim 11: The method of claim 10, further comprising:

adjusting the number of sticks stacked together in the layout to fit within a scanner view field.

Claim 12: The method of claim 1, further comprising:

in-line inspecting the test chip using an optical inspection tool.

Claim 13: The method of claim 1, wherein the test chip includes a plurality of design pattern variations.

Claim 14: The method of claim 1, wherein the test structures are two-terminal or four-terminal test structures.

Claim 15: The method of claim 1, wherein one of the test structures is a snakecomb cell configured to localize a defect in the snakecomb cell to a location within the snakecomb cell.

Claim 16: The method of claim 1, wherein electrically testing includes:

comparing a line resistance to a first threshold resistance, wherein the line resistance is determined based on a measured voltage;

when the line resistance is below the first threshold voltage, detecting a soft short;

comparing the line resistance to a second threshold resistance; and

when the line resistance is below the second threshold resistance, detecting a hard short, wherein the first threshold resistance is greater than the second threshold resistance.

Claim 17: The method of claim 1, wherein electrically testing includes:

determining an average resistance for a number of lines adjacent to each other;

comparing a line resistance to the average resistance;

when the line resistance is less than the average resistance by a first specified amount, detecting a soft short; and

when the line resistance is less than the average resistance by a second specified amount, detecting a hard short, wherein first specified amount is less than the second specified amount.

Claim 18: The method of claim 1, wherein the parallel electrical tester is connected to a wafer loader and a wafer prober, and further comprising:

loading one or more test chips from the wafer loader into the wafer prober to be tested, and wherein the wafer prober includes a probe card to electrically contact the test structures on the test chip to be electrically tested in parallel.

Claim 19: The method of claim 18, further comprising:

transmitting test signals between the probe card and a pin termination module in the parallel electrical tester;

transmitting test signals between the pin termination module and a measurement control module in the parallel electrical tester; and

transmitting commands to the wafer prober from a tester control module in the parallel electrical tester.

Claim 20: The method of claim 19, further comprising:

providing voltage sources and transmitting control signals from the measurement control module to the pin termination module.

Claim 21: The method of claim 19, further comprising:

receiving test signals from the probe card at a plurality of switch cards in the pin termination module, wherein each switch card is connected to a group of pins from the probe card.

Claim 22: The method of claim 21, wherein a switch card forms a resistor divider with a resister in a test structure, a termination resistor, and a voltage source.

Claim 23: The method of claim 21, wherein a switch card includes:

a plurality of pin terminator circuits, wherein each pin terminator circuit is connected to a pin from the probe card; and

a plurality of digital multiplexer controls, wherein each digital multiplexer control is connected to two pin terminator circuits.

Claim 24: The method of claim 23, wherein a pin terminator circuit includes a plurality of quad switches, wherein each quad switch is connected to a voltage source and control signals.

Claim 25: The method of claim 19, further comprising:

receiving test signals from the probe card at a multiplexer module in the measurement control module;

combining a set of test signals received from the probe card into a digital acquisition signal; and

transmitting the digital acquisition signal to a digital acquisition card.

Claim 26: The method of claim 1, wherein analyzing results comprises:

classifying detected defects as random or systematic defects.

Claim 27: The method of claim 26, further comprising:

grouping test chip design patterns into layout bins; and

plotting failure counts for each layout bin.

Claim 28: A system for fast localization of electrically measured defects of integrated circuits, comprising:

(a) a test chip having test structures configured to be parallel electrically tested, wherein the test structures are grouped into one or more padgroups, wherein the test structures in a padgroup are electrically tested together in parallel;

(b) a parallel electrical tester configured to parallel electrically test the test structures on the test chip; and

(c) a processor configured to analyze results from the parallel electrical tester to localize defects on the test chip.

Claim 29: The system of claim 28, further comprising:

an inspection tool configured to inspect the localized defects on the test chip.

Claim 30: The system of claim 29, wherein the inspection tool is a scanning electron microscope (SEM).

Claim 31: The system of claim 30, wherein the test structures on the test chip are sized to be compatible with a view field of the SEM.

Claim 32 (Canceled)

Claim 33: The system of claim 28, wherein a padgroup includes:

two columns of test structures; and

two columns of pads disposed between the two columns of test structures.

Claim 34: The system of claim 28, wherein padgroups are grouped into one or more sticks, wherein the padgroups in a stick are electrically tested together in parallel.

Claim 35: The system of claim 34, wherein the padgroups in a stick are electrically tested together in parallel using a probe card connected to the parallel electrical tester.

Claim 36: The system of claim 35, wherein one or more cells having test structures and corresponding pads are disposed between two padgroups in a stick, wherein the one or more cells are used to verify the operation of the probe card.

Claim 37: The system of claim 34, wherein two or more sticks are stacked together in a layout.

Claim 38: The system of claim 37, wherein the number of sticks stacked together in the layout is adjusted to fit within a scanner view field.

Claim 39: The system of claim 28, further comprising:

an optical inspection tool to in-line inspect the test chip.

Claim 40: The system of claim 28, wherein the test chip includes a plurality of design pattern variations.

Claim 41: The system of claim 28, wherein the test structures are two-terminal or four-terminal test structures.

Claim 42: The system of claim 28, wherein one of the test structures is a snakecomb cell configured to localize a defect in the snakecomb cell to a location within the snakecomb cell.

Claim 43: The system of claim 28, wherein test structures are placed at more than one level.

Claim 44: The system of claim 43, wherein test structure below a test structure on another level is electrically tested.

Claim 45: The system of claim 43, wherein the interaction of test structures at two different levels is measured.

Claim 46: The system of claim 28, wherein the parallel electrical tester is configured to:

compare a line resistance to a first threshold resistance, wherein the line resistance is determined based on a measured voltage;

when the line resistance is below the first threshold voltage, detect a soft short;

compare the line resistance to a second threshold resistance; and

when the line resistance is below the second threshold resistance, detect a hard short, wherein the first threshold resistance is greater than the second threshold resistance.

Claim 47: The system of claim 28, wherein the parallel electrical tester is configured to:

determine an average resistance for a number of lines adjacent to each other;

compare a line resistance to the average resistance;

when the line resistance is less than the average resistance by a first specified amount, detect a soft short; and

when the line resistance is less than the average resistance by a second specified amount, detect a hard short, wherein first specified amount is less than the second specified amount.

Claim 48: The system of claim 28, wherein the parallel electrical tester is connected to a wafer loader and a wafer prober, wherein the wafer loader loads one or more test chips into the wafer prober to be tested, and wherein the wafer prober includes a probe card to electrically contact the test structures on the test chip to be electrically tested in parallel.

Claim 49: The system of claim 48, wherein the parallel electrical tester includes:

a pin termination module connected to the probe card, wherein test signals are transmitted between the pin termination module and the probe card;

a measurement control module connected to the pin termination module, wherein test signals are transmitted between the pin termination module and the measurement control module; and

a tester control module connected to the measurement control module and the wafer prober, wherein the tester control module sends commands to the wafer prober.

Claim 50: The system of claim 49, wherein the measurement control module provides voltages source and control signals to the pin termination module.

Claim 51: The system of claim 48, wherein the pin termination module includes:

a plurality of switch cards to receive test signals from the probe card, wherein each switch card is connected to a group of pins from the probe card.

Claim 52: The system of claim 48, wherein a switch card forms a resistor divider with a resister in a test structure, a termination resistor, and a voltage source.

Claim 53: The system of claim 51, wherein a switch card includes:

a plurality of pin terminator circuits, wherein each pin terminator circuit is connected to a pin from the probe card; and

a plurality of digital multiplexer controls, wherein each digital multiplexer control is connected to two pin terminator circuits.

Claim 54: The system of claim 53, wherein a pin terminator circuit includes a plurality of quad switches, wherein each quad switch is connected to a voltage source and control signals.

Claim 55: The system of claim 49, wherein the measurement control module includes:

a multiplexer module that receives test signals from the probe card; and

a digital acquisition card, wherein the multiplexer module combines a set of test signals received from the probe card into a digital acquisition signal sent to the digital acquisition card.

Claim 56: The system of claim 28, wherein the processor is configured to:

classify detected defects as random or systematic defects.

Claim 57: The system of claim 56, wherein the processor is configured to:

group test chip design patterns into layout bins; and

plot failure counts for each layout bin.

Claim 58: A computer-readable storage medium containing computer executable code to instruct a computer to localize electrically measured defects of integrated circuits by instructing the computer to operate as follows:

sending control signals from a parallel electrical tester to a test chip fabricated to have test structures configured for parallel electrical testing, wherein the test structures are grouped into one or more padgroups, wherein the test structures in a padgroup are electrically tested together in parallel; and

analyzing results of the electrical testing to localize defects on the test chip.